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A Comparison of RFIC Fabrication Technologies

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This tutorial provides a brief overview of the capabilities and limitiations of major integrated circuit technologies used for RF and other high frequency devices

Continued growth in wireless, optical and other high-speed, high-frequency products has created a demand for integrated circuits that are optimized for performance, cost and practical development complexity. These radio-frequency ICs (RFICs) represent a wide range of requirements that continues to be met with an equally wide range of solutions, from low-cost ubiquitous CMOS to advanced III-V materials.

In this tutorial, we'll take a look at the major IC fabrication processes used for RFICs. Although there are variations among the various facilities, there are general performance ranges that each process fits into. Hopefully, this note will provide an introductory-level understanding of the choices an engineer must make when choosing the right process to manufacture the device required for the end product being developed.

Fortunately for that engineer, the demand and the range of performance required has resulted in some innovative advancements in IC design and fabrication. We will try to make note of as many specific features as possible as we review the various processes.

RFICs in CMOS

Complementary metal-oxide semiconductor (CMOS) processes are the cheapest, offering high yields, large wafer size, and many fabs with years of experience making ICs of all types, from millions of computer memory chips to general-purpose analog and digital building block devices. The raw material is cheap and the volume of work in the digital realm has already brought down the cost of fabrication to rock bottom.

However, the challenges for making high-frequency ICs in silicon have been enormous. When first explored for RFICs, CMOS was the worst available process for noise performance, passive component integration, electrostatic discharge (ESD), and device modeling. Concentrated research efforts have dramatically reduced the performance gap between CMOS and other popular processes such as silicon BiCMOS or its SiGe variant.

CMOS has performance advantages in addition to the obvious cost advantage. First, it's digital heritage has made new RF CMOS processes a logical choice (pun intended) for high-speed digital circuitry, including important RF building blocks such as frequency synthesizers and oscillators, switches and baseband processors. Driven by the computing industry and Moore's Law, geometries of 0.18 µm allow higher frequency operation simply through reduction in physical size. These small features also reduce power consumption, but at a cost in noise performance and signal handling capability.

CMOS is promising for future RFICs with even more ambitious cost/performance demands. Because this process has improved by such a dramatic amount in a relatively short time, it has many supporters in the RFIC development community.

SiGe BiCMOS and HBT

This process was chosen next, because of its balance among performance, cost and complexity. Making SiGe RFICs in the fab is only a small degree more difficult than ordinary

silicon CMOS, bipolar and BiCMOS processes. The initial difficulty was in the development of consistent doping profiles and accurate design and process modeling tools. These kept the cost of SiGe high for a time.

Current SiGe heterojunction bipolar transistor (HBT) technology offers F_T competitive with GaAs, the first real microwave IC technology, although GaAs still offers better integration of passives and better power-handling capability. When high frequency operation with very good noise performance, mixed-signal capability, and low cost/high volume manufacturing, SiGe is often the process of choice.

GaAs and other III-V Semiconductors

For overall performance in microwave circuits, compound semiconductors have significant performance advantages. The design of the circuit and its implementation on the IC substrate are simpler than with the silicon-based processes. As noted above, power handling and on-chip passives, particularly inductors, is superior to the other processes. An early drawback was in modeling. Traditional IC processes relied on time-domain (SPICE) analysis of the circuit to verify its performance in final form, fabricated on a semiconductor substrate. With microwave circuits used on GaAs, the distributed elements and passive components could not be accurately modeled in the time domain. As a result, GaAs evolved along a modeling path that was distinct from silicon processes. This caused an "either/or" approach within entire companies, and gave rise to GaAs specialized tools that had no use in the silicon realm. Only recently have the barriers between the process types been removed, as the simulation and modeling tools became more comprehensive.

GaAs has improved with time, as have all the other available processes. Costs have been reduced and the recent increase in the use of pHEMT technology has provided a performance enhancement, restoring the high-frequency advantages that seemed to be eroding as SiGe was developing.

GaAs is often the preferred process for higher frequencies, lowest noise, and highest power, compared to the other available processes. Various other III-V semiconductor processes allow even higher frequency operation and other performance advantages.

Other Processes

Classic silicon bipolar and BiCMOS are still very popular, given their maturity and low cost. Below 1 GHz, silicon BiCMOS is probably the most-used process for IF signal processing, high-speed operational amplifiers and data conversion products. Where standard digital functionality is less important, low cost silicon bipolar technology is used more often than many industry observers might expect.

Silicon-on-insulator (SOI, also silicon-on-glass or silicon-on-sapphire) is an interesting CMOS or BiCMOS process, where the traditional silicon substrate is thinned and mounted to a supporting insulating layer. This configuration results in very high isolation between circuit elements and reduces noise. Both of these characteristics are important for RF circuits, and SOI is used for low noise phase-locked loops and high-isolation analog and RF switches.

Design Tools

Finally, none of the advances in any IC process would be possible without a parallel advance in software for the design, layout, simulation and verification of the device. Foremost among the advances has been a steady merging of classic RF/microwave circuit design tools and IC design, layout and verification tools. Although this process is not complete, nearly all of the former barriers have been removed—the circuit design software can share data easily with the IC design software.

Any engineer beginning the process of design that will result in an RFIC solution must understand both the fabrication process and the modeling tools that will be used to design the circuit and create its IC implementation.